In the claims:

The following is a full listing of claims as originally filed or most recently amended.

Claim 1. (Previously Presented) An integrated circuit including an embedded memory and a built-in self-test arrangement comprising

means for storing test instructions and discriminating between performing manufacturing level or board level testing and system level testing based on receiving test instructions provided from an external tester,

means for generating default test instructions for performing system level testing when test instructions are not provided by said external tester, and

means for supplying said default test instructions for performing system level testing to said means for storing test instructions,

wherein said means for generating default test instructions includes an initialization storage means for providing signals for initializing said means for storing test instructions in the absence of said test instructions provided from an external tester.

Claim 2. (Canceled)

Claim 3. (Previously Presented) An integrated circuit as recited in claim 1, wherein said initialization storage means is a storage initialization module.

Claim 4. (Original) An integrated circuit as recited in claim 1, further including

means for activating said means for generating said default test instructions responsive to an absence of test instructions from an external tester.

Claim 5. (Original) An integrated circuit as recited in claim 1, further including

means for controlling a test operation, wherein said means for controlling a test operation includes means for supplying a control signal to an instruction storage controller and further includes said means for storing said test instructions.

Claim 6. (Previously Presented) An integrated circuit as recited in claim 5, further including

means for activating said means for generating said default test instructions when only said control signal is supplied to said instruction storage controller.

Claim 7. (Original) An integrated circuit as recited in claim 1, wherein said means for generating default test instructions includes a memory for storing said default test instructions.

Claim 8. (Previously Presented) An electronic system including an integrated circuit having a built-in self-test arrangement therein, said integrated circuit comprising

means for storing test instructions and discriminating between performing manufacturing level or board level testing and system level testing based on receiving test instructions provided from an external tester,

means for generating default test instructions for performing system level testing in absence of instructions from an external tester, and

means for supplying said default test instructions for performing system level testing to said means for storing test instructions, wherein said means for generating default test instructions includes an initialization storage means for providing signals for initializing said means for storing test instructions in the absence of said test instructions provided from an external tester.

Claim 9. (Canceled)

Claim 10. (Previously Presented) A system as recited in claim 8, wherein said initialization storage means is a storage initialization module.

Claim 11. (Original) A system as recited in claim 8, further including

means for activating said means for generating said default test instructions responsive to an absence of test instructions from an external tester.

Claim 12. (Previously Presented) A system as recited in claim 8, further including

means for controlling a test operation, wherein said means for controlling a test operation includes means for supplying a control signal to an instruction storage controller for providing signals for initializing said means for storing said test instructions.

Claim 13. (Original) A system as recited in claim 12, further including

means for activating said means for generating said default test instructions when only said control signal is supplied to said instruction storage controller.

Claim 14. (Original) A system as recited in claim 12, wherein said control signal is supplied from an external tester.

Claim 15. (Original) A system as recited in claim 12, wherein said control signal is supplied from within said system.

Claim 16. (Original) A system as recited in claim 8, wherein said means for generating default test instructions includes a memory for storing said default test instructions.

Claim 17 (Previously Presented). A method of performing system level tests on an electronic system including an integrated circuit having a built-in self-test (BIST) arrangement therein for performing manufacturing level or board level testing and including means for storing a test algorithm, said method comprising steps of

discriminating a source of a test command,

providing a system level test algorithm from said BIST arrangement in absence of instructions from an external tester,

transferring said system level test algorithm to said means for storing a test algorithm in said BIST arrangement, and

operating said BIST arrangement using said system level test algorithm.